IN THE CLAIMS

1 - 11 Canceled

12. (Currently Amended) A method of forming a capacitor on a semiconductor substrate together with an integrated circuit comprising a plurality of first type circuit devices and a plurality of second type circuit devices, the method including the steps of:

(a) concurrently forming a capacitor device body and a plurality of first type device bodies in the semiconductor substrate using a first type of dopant material, each first type device body corresponding to a respective one of the first type circuit devices;

(b) concurrently forming a dielectric layer over the capacitor device body and over each first type device body;

(c) concurrently forming an electrode layer over the dielectric layer in an area defined by an upper surface of the capacitor device body and in each respective area defined by an upper surface of each respective first type device body;

(d) forming a first lateral region and a second lateral region in the semiconductor substrate along opposite lateral sides of the capacitor device body and concurrently forming a respective drain region and a respective source region in the semiconductor substrate for a number of the second type circuit devices, the first lateral region and second lateral region being formed using the first type of dopant material at a level relatively higher than is characteristic of the capacitor device body;

(e) forming an insulating layer over the electrode layer, first lateral region, second lateral region, each respective drain region, and each respective source region;

(f) electrically connecting the first and second lateral regions to a first supply voltage

potential at a first longitudinal end of the capacitor device body; ~~and~~

(g) electrically connecting the electrode layer situated over the upper surface of the capacitor device body to a second supply voltage potential at a second longitudinal end of the capacitor device body opposite to the first longitudinal end of the capacitor device body;

(h) forming a buried oxide layer in the semiconductor substrate, the buried oxide layer being formed in an area for the capacitor and in a respective area for each respective circuit device;

(i) forming a first set of side oxide regions in the semiconductor substrate for the capacitor, the first set of side oxide regions bounding the area for the capacitor;

(j) forming a respective additional set of side oxide regions in the semiconductor substrate for each respective circuit device, the respective additional set of side oxide regions bounding the area for the respective circuit device; and

(k) wherein the steps of forming the buried oxide layer and each set of side oxide regions are performed prior to forming the capacitor device body and each first type device body.

13. Canceled

14. (Original) The method of Claim 12 wherein the step of forming the first lateral region, second lateral region, each drain region, and each source region also includes concurrently forming a first end region in the semiconductor substrate abutting the first longitudinal end of the capacitor device body and contacting the first and second lateral regions adjacent to the first longitudinal end of the capacitor device body.

15. Canceled

16. (Currently Amended) The method of Claim ~~15~~ 12 wherein the first type of dopant material comprises N-type material and the step of forming the capacitor device body and each first type device body includes implanting the N-type material in the areas of the semiconductor substrate defined within each respective set of side oxide regions corresponding to the capacitor device body and each first type device body.

17. (Previously Amended) The method of Claim 16 wherein the step of forming the first lateral region and second lateral region comprises implanting additional N-type material in areas defined between lateral sides of the capacitor device body and the first set of side oxide regions, and wherein the step of forming each drain region and each source region comprises implanting N-type material for the respective second type circuit devices.

18. (Previously Amended) A method for improving the frequency response of a decoupling capacitor in an integrated circuit, the decoupling capacitor including a device body analogous to the device body of a first type of transistor included in the integrated circuit and being formed using a first type impurity material, the decoupling capacitor further including first and second lateral regions analogous to the source and drain regions of a second type of transistor included in the integrated circuit chip, the method comprising the step of:

(a) adding additional first type impurity material to an area in the substrate for the decoupling capacitor device body located above a buried oxide layer of a silicon-on-insulator integrated circuit, the additional first type impurity material resulting in a region on the substrate for the decoupling capacitor device body that is more

highly doped than a region on the substrate for the first type of transistor device body.

19. Canceled

20. Canceled